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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,253	11/12/2003	Junichi Amada	02410281US	3191

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EXAMINER	
WILLOUGHBY, TERRENCE RONIQUE	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,253	AMADA ET AL.	
	Examiner	Art Unit	
	Terrence R. Willoughby	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 and 3 is/are rejected.

7)☒ Claim(s) 2 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/12/03;11/10/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Junichi et al. (JP 11205114) in view of Bober (US 5,625,518) and in further view of Glidden et al. (US 6,493,204).

Regarding claim 1, Junichi et al. discloses an electric parts drive circuit (Fig. 2) comprising: a first field-effect transistor (10) for allowing an electric current flow into a plus line and provided between the plus line to be connected to a plus terminal (Tc) of a battery (BT) and an electric part (L) and (paragraph [0002], lines 5-10); a second field-effect transistor (30) including in parallel a second parasitic diode (20) for allowing an electric current flow from the first field–effect transistor (10) into the electric part (L), the first field-effect transistor (10) and the second field-effect transistor (30) being connected in series (Fig. 2, numerals 10 and 30) in order from the plus line (Tc) to the electric part(L); a third field-effect transistor (60) for allowing an electric current flow into the electric part (L) and provided between a minus line to be connected to a minus terminal (Td) of the battery (BT) and the electric part (L), see (Abstract). The first and

third field-effect transistors do not eachshow a parasitic diode in parallel respectively with the first (10) and third (60) field-effect transistors however, it is well known to those skilled in the art at the time the invention was made to use a parasitic diode in parallel with a field-effect transistor, such as the second field-effect transistor (30) including in parallel a parasitic diode (20) taught by Junichi et al. to prevent potential damage to a drive circuit, by blocking the electric current flow from the power source to a inductive load, such as a solenoid. Junichi et al. lacks a reverse connection protection for the second field-effect transistor (30).

However, Bober discloses a reverse connection protection (Fig. 1, numeral 26) for a second field-effect transistor (Fig. 2, numeral 62) and (Column 3, lines 30-33). It would have been obvious to those skilled in the art at the time the invention was made to provide a reverse connection protection taught by Boberto the electric parts drive circuit of Junichi et al. to provide reverse polarity protection when the power source is connected mistakenly in the wrong manner to prevent major potential damage to the electric part drive circuit.

Both Junichi et al. and Bober lack a failure diagnosis switch for switching between conduction and shutoff between the drain of a second field-effect transistor and the plus terminal of the battery; and a switch control unit for controlling switching between conduction and shutoff of the first to third field-effect transistors and the failure diagnosis switch unit, wherein the switch control unit diagnoses a failure of the second

field-effect transistor based on the voltage between the first and second field-effect transistors responsive to switching between conduction and shutoff of the second field-effect transistor in a state that the first and third field-effect transistors are shut off and the failure diagnosis switch unit is brought into conduction.

However, Glidden et al. discloses a failure diagnosis switch unit (Column 3, 30-47) for switching between conduction and shutoff between the drain of a MOSFET transistor (Fig. 11, numeral 44) and a switch control unit (Fig. 11, numeral 35) for controlling switching between conduction and shutoff (Column 2, lines 24-30) and having a control port being responsive to a control voltage applied to the control port (Column 3, lines 6-29). It would have been obvious to those skilled in the art at the time the invention was made to provide a failure diagnosis switch unit taught by Glidden et al. between the drain of the second-field effect transistor and the plus terminal of the battery of Junichi et al. and Boder circuit and a switch control unit for controlling switching between conduction and shutoff taught by Glidden et al. of the first to third field-effect transistors and the failure diagnosis switch unit taught by Junichi et al. and Boder circuit, wherein the switch control unit diagnoses a failure of the second field-effect transistor based on the voltage between the first and second field-effect transistors responsive to switching between conduction and shutoff of the second field-effect transistor in a state that the first and third field-effect transistors are shut off and the failure diagnosis switch unit is brought into conduction to assure that the electronic

switch is functionally working between the conduction and shutoff states providing better control of the solenoid valve in the anti-lock brake system.

Regarding claim 3, Junichi et al. in view of Bober and in further view of Glidden et al. discloses the electric parts drive circuit as set forth in claim 1, wherein the electric part is a solenoid in an electromagnetic valve of a brake fluid pressure controller for a vehicle.

Allowable Subject Matter

3. Claim 2 is objected to as being dependent upon a rejected base claim 1, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Combined claim 2 would be allowable over the art of record because the prior art does not teach the failure diagnosis switch unit comprising: a PNP transistor having a connector connected via a first resistor between the plus terminal of the battery and the drain of the second field-effect transistor; second resistors and an NPN transistor connected in series between the plus terminal of the battery and ground; and third resistors connected in series between the switch control unit and ground, wherein the connection point of the second resistors is connected to the base of the PNP transistor

and the connection point of the third resistor is connected to the base of the NPN transistor as set forth in the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRW

PHUONG T. VU
PRIMARY EXAMINER